Scanning Probe Microscopy for Site Specific Defect Localization in FinFET Devices

Nirmal Adhikari, PhD

GlobalFoundries, Essex Junction, VT, USA
nirmal.adhikari@globalfoundries.com

Scanning Capacitance Microscopy (SCM) has proven itself as a critical technique for finding and understanding three dimensional dopant related root cause mechanisms. Three-dimensional device architectures in advanced node technology such as fin field-effect-transistors (FinFET) , requires an analytical technique to map the dopant and carrier distributions accurately as their vertical positioning in the source/drain (S/D), channel, conformality and absolute concentration affects the device performance. In addition, physical failure analysis of FinFET devices frequently reaches a "dead end" with a No Defect Found (NDF) result when channel doping issues are the suspected culprit (e.g., high VTH, low VTH, low gain, sub-threshold leakage, etc.). In new technology development, the lack of empirical dopant profile data to support device and process models and engineering has had, and continues to have, a profound negative impact on these emerging technologies. Therefore, there exists a critical need for dopant profiling in the industry to support the latest technologies that use FinFET as their fundamental building block. Location-specific (i.e., specific fin) SCM doping profile of FinFET devices has not been resolved spatially before to individual fins level, therefore many challenges exist. Some of the critical issues are need of highly controllable material removal, SCM spatial resolution to accurately resolve the defect and strength of the doping signal. Here, we present the novel sample preparation techniques and analysis for advanced node FinFET devices using scanning probe microscopy (SPM).

Context microscopy and spectroscopy to advance semiconductor devices – conductive AFM linked to a wealth of other analytical techniques via nanoGPS technology

Prof. Silke H. Christiansen
Fraunhofer Institute for ceramic technologies and systems – IKTS, Äussere Nürnbergerstr. 62, 91301 Forchheim, Germany
Freie Universität Berlin, Arnimallee 14, 14195 Berlin, Germany
silke.christiansen@ikts.fraunhofer.de

The design complexity of electronic components and the heterogeneity of new materials constantly increase with decreasing device sizes even down to the nanometer scale. Engineering of novel devices will account for a high level of reliability, sustainability, and longevity as part

of quality standards which have to be met. In the related device optimization endeavor the detection and classification of nanoscale material imperfections as well as scale bridging material and device properties will be success critical and require the use of complementing analytical methods.
Here, the true correlation of electron- ion-, optical- and x-ray microscopy and complementing spectroscopies (optical, mass) is constantly emerging including the use of atom probe techniques in this analytical context. To account for truly correlative analytics, the application of the nanoGPS technology is an enabler when rigorously be applied for the aforementioned analytical modalities.
We will demonstrate the use of the nanoGPS technology to correlate analytical and imaging modalities for selected examples of silicon based ASICs. The underlying preparative and consecutive analytical workflows will be demonstrated. In addition, we will show the application of machine learning strategies to aforementioned heterogeneous data to further improve efficient material and device optimization.

Enabling electrical SPM for advanced nanoelectronics device characterization

Thomas Hantschel, PhD

imec, Materials and Components Analysis Department
Scanning Probe Microscopy Team
thomas.hantschel@imec.be

Scanning probe microscopy (SPM) has become an indispensable tool for the development of next generations of nanoelectronics devices given the achievable nanometre spatial resolution and its high versatility to probe a broad range of signals (e.g. topography, electrical properties, magnetic fields, temperature). This talk concentrates on the use of dedicated SPM methods for the nanoscopic electrical characterization of semiconductor device structures. The scanning spreading resistance microscopy (SSRM) method is discussed which supports the development and fine tuning of advanced fabrication nodes by measuring the carrier concentration inside transistor device structures with 1 nanometre spatial resolution in a quantitative manner. Furthermore, the conductive AFM (CAFM) approach is presented which helps us to study and understand the formation mechanism of nanoscopic filament structures in advanced memory structures. We show that the establishment of high-performance conductive diamond tips and the development of SPM nanotomography have been two important enablers for these advances. Finally, we introduce the promising reverse tip sample (RTS) configuration which overcomes the single-tip limitation of conventional SPM.

SPM challenges of semiconductor failure analysis

Dr. Andreas Altes
Infineon Technologies AG
Am Campeon 1-1285579 Neubiberg, Germany
andreas.altes@infineon.com

Miniaturized and integrated semiconductor devices provide good opportunities to benefit from modern SPM capabilities in order to investigate its characteristics down to the nm-scale. Next to the investigation of topography and roughness at various surfaces during the process of production especially the 2D analysis of doping type and doping concentration within active area of Si is of high interest at manufacture of semiconductors. Hereby the well-known common methods like SCM and SSRM are applied frequently. Basic requirement for obtaining conclusive measurements is the usage of an reliable and stable SPM equipment, which is easy to operate and comfortable in usage. In addition to the pure scan procedure, which is just a small part somewhere in the middle of the entire SPM analysis flow, there is quite a lot of effort to spend for preliminaries and post processing. This is all the more valid if there is just one „golden sample“ available for analysis. Within this presentation – using an SSRM analysis as an example - it is demonstrated how a systematic and sophisticated approach will finally lead to a successful SPM analysis which in turn results into helpful conclusions. By pointing out particular challenges it is also shown how important it is to continue on further method development in order to fulfill requirements of new technologies with even smaller scales. Thus, further improvements of achievable spatial resolution, sensitivity and stability by using e.g. vacuum conditions are just as well desired as methods for determination of quantitative doping concentration by using e.g. SMM or sMIM.

Exploring dynamic charging processes in semiconductor devices using time-resolved Kelvin probe force microscopy

Ilka M. Hermes
Park Systems Europe GmbH, Schildkrötstrasse 15, 68199 Mannheim, Germany
ihermes@parksystems.com

Daniel Sommer
United Monolithic Semiconductors GmbH,
Wilhelm-Runge-Straße 11, Ulm, Germany
Daniel.Sommer@ums-rf.com

Trap-related phenomena in semiconductor devices can limit device performances significantly. Here, a spatial- and time-resolved visualization of the charge distribution inside electronic devices upon electrical excitation can give valuable insights on these phenomena and aid to eliminate performance bottlenecks. Adapting to ever decreasing device dimensions, Kelvin probe force

microscopy (KPFM) resolves charge and potential distributions with a nanometer resolution.[1] In particular, frequency modulated (FM) KPFM methods, like sideband KPFM, have shown the highest spatial resolution and electrical accuracy.[2]
In this study, we investigated dynamic charging and draining processes on GaN-based high electron mobility transistors (HEMTs) with varying device passivation. Different operation conditions of the coplanar devices are obtained by actively modulating the gate and drain voltage while drain and gate current are monitored. Simultaneously, a line-by-line sideband KPFM approach acquired the spatial-and time-resolved surface potential distributions across the gate-drain channel. The potential signals revealed dissimilarities between in electric field distribution and build-up depending on the dielectric material used for surface passivation – a result that may be linked to the device behaviour during reliability tests. Furthermore, we found that after switching, some transistors exhibited a slow charge drain over several minutes in their potential response, which could be caused by a slow redistribution of trapped charges located in or nearby the surface of the gate-drain area.

[1] Melitz, W.; Shen, J.; Kummel, A. C.; Lee, S. Kelvin probe force microscopy and its application. Surf. Sci. Rep. 2011 66, 1–27.
[2] Axt, A.; Hermes, I. M.; Bergmann, V. W.; Tausendpfund, N.; Weber, S. A. L. Know your full potential: Quantitative Kelvin probe force microscopy on nanoscale electrical devices. Beilstein J. Nanotechnol. 2018 9(1), 1809-1819.